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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,377	08/29/2001	Hansel A. Collins	TRIC-1	9695

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EXAMINER
TABONE JR, JOHN J

ART UNIT	PAPER NUMBER
2133	2

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DATE MAILED: 03/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/942,377	COLLINS, HANSEL A.	
	Examiner	Art Unit	
	John J Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,19 and 20* is/are rejected.

7)☒ Claim(s) *13-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been examined.

Specification

2. The disclosure is objected to because of the following informalities: On page 8 line 16, warn should be changed to warm. Appropriate correction is required.

Claim Objections

3. Claims 7, 9 and 15 are objected to because of the following informalities:

Claim 7:

Line 2, warn should be changed to warm. Appropriate correction is required.

Claim 9:

Line 5, DCS should be changed to DSC. Appropriate correction is required.

Claim 15:

Claim 15 ends in two periods. Appropriate correction is required.

4. Claims 13-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an Examiner's Statement of Reasons for Allowance:

The prior arts of record teach A plurality of DSC Data Channels and a DSC Clock Channel (see claim 12 rejection, under item 8); Collins et al. (US-6031847) is one example of such prior arts. The prior arts of record, however, fail to teach, singly or in

combination, the details of the DSC Clock Channel as disclosed in claims 13 and 14. Claims 15-18 continue to disclose further details of the DSC Data Channel that are taught by the prior arts of record. The Examiner asserts that the novelty of the claim, when read as a whole, is: the system of claim 12 wherein the DSC Clock channel comprises a Clock Channel Front-End block, Built-In Self-Test Logic, and a utility block. The Clock Channel Front-End block comprises a finite state machine, Clock Image Latch, Image Decode Logic, String-to-Binary Encoder circuit, DNA logic block, Delay Line, Trim Delay Circuit, and glue logic. Also, each DSC Data Channel comprises a Data Channel Front-End block, Data FIFO, and utility block. The Data Channel Front-End block comprises a finite state machine, Data Image Latch, Image Decode Logic, String-to-Binary Encoder circuit, DNA logic block, Delay Line, Trim Delay Circuit, and glue logic. The Data FIFO comprises a Pattern Search finite state machine, Data FIFO Register File, FIFO Address Encoder, Write Pointer, Read Pointer, Frame Bit Counter, and Skew Synchronizing Marker Start Sequencer. The Data FIFO Register File is a write-per-bit FIFO.

Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 3, 19 and 20 are rejected under 35 U.S.C. 112, second paragraph, for lack of antecedent basis.

Claim 3:

Claim 3 recites the limitation " link clock switching by holding the link clock signal" in claim 1. There is insufficient antecedent basis for this limitation in the claim.

Claims 19 and 20:

Claims 19 and 20 recites the limitation "DSC bundle" in claim 12. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Collins et al. (US-6031847).

Claim 1:

"a. sending a training sequence from a source to a receiver across the parallel data channels...;"

Collins teaches in step 1302, the transmitter (e.g., transmitter 301) sends a training micropacket as part of an initial training sequence which includes a training detect sequence, a flush sequence, and a ping sequence. (See col. 14, lines 20-24).

"b. detecting the link-reset signature for a minimum specified amount of time...;"

Collins teaches the flush sequence is 14 ns long, and functions by flushing the delay lines of the respective delay stacks 310-313 with logical zeros in preparation for the ping sequence. (See col. 11, lines 14-16).

"c. performing delay path calibration for the clock channel;"

Collins teaches of a two step clock edge placement which includes measuring the clock period and clock offset. (See col 12, lines 35-37, 44-46).

"d. performing link skew compensation;"

Collins teaches each of the communications channels (e.g., channels 0-3) are coupled to the delay stack structure 303, where they are individually "programmed" to insert the proper amount of delay for skew compensation. (See col. 7, lines 48-51).

"e. ... providing word alignment ..."

Collins teaches the provision of word alignment by system 300, which removes the skew from the individual bits comprising each of the received data words. (See col. 6, lines 39,40 and col. 7, lines 33-35).

Claim 2:

"... the plurality of data channels is scalable."

Collins teaches scalability in that the four channels 0-3 of system 300 form a portion of a high performance parallel interface (HIPPI) data transmission system. Collins discloses that system 300, which implements a HIPPI compliant data transfer system, actually includes 22 communications channels in each direction, for a total of 44 communications channels. Collins further suggests that while the present embodiment is implemented in accordance with the HIPPI specification, it should be appreciated that the method and system of the present invention is suited to use with other parallel data transmission protocols (i.e. small computer system interface (SCSI) datra transmission and reception systems). (See col. 6, lines 45-67, col. 7, lines 1-11).

Claim 3:

"the link-reset signature is produced by stopping the link clock switching by holding the link clock signal at either a logical one or logical zero state."

Collins teaches in normal micropackets the Frame signal is high for the first 20 ns of the period and low for the last 20 ns, while the CLK signal alternates every 2 ns. During the first portion of the training micropacket (flush sequence), however, CLK is driven high for 6 ns and then driven low, while Frame is alternately driven high and low every 2 ns. In this, Collins discloses the procedure of holding the CLK signal for a period of time (i.e. 6ns) to a logical one or zero state.

Claim 4:

"a. sending a second training sequence...;"

Collins teaches in step 1303, the transmitter sends another training micropacket to retrain each of the delay stacks. This second training micropacket is sent immediately after the first training micropacket sent in step 1302. (See col. 11, lines 37-40).

"b. ... providing word alignment...;"

Collins teaches the provision of word alignment by system 300, which removes the skew from the individual bits comprising each of the received data words. (See col. 6, lines 39,40 and col. 7, lines 33-35).

Claim 5:

Collins teaches at system 300 power up, transmitter 301 sends normal micropackets alternating with training micropackets (cold training sequence) until receiver 302 is properly trained and is ready for normal operation. (See col. 14, lines 1-3).

Claim 6:

"b. immediately initiating a second training sequence."

Collins teaches in step 1303, the transmitter sends another training micropacket to retrain each of the delay stacks. This second training micropacket is sent immediately after the first training micropacket sent in step 1302. (See col. 14, lines 37-40).

"a. causing a link reset such that the data channels are reset and all calibration values obtained during a previous training sequence are cleared;"

Collins teaches of a flush sequence (link reset) which has the function of flushing the delay lines of the respective delay stacks with logical zeros. (See Collins col. 11, lines 14-16).

Claim 7:

"a. sending a training sequence ...;"

Collins teaches in step 1302, the transmitter (e.g., transmitter 301) sends a training micropacket as part of an initial training sequence which includes a training detect sequence, a flush sequence, and a ping sequence.

"b. ... providing word alignment...;"

Collins teaches the provision of word alignment by system 300, which removes the skew from the individual bits comprising each of the received data words. (See col. 6, lines 39,40 and col. 7, lines 33-35).

"c. in accordance with the command sequence, sending multiple command bytes;"

Collins teaches in step 1302, the transmitter (e.g., transmitter 301) sends a training micropacket as part of an initial training sequence. (See col. 14, lines 20-24). A "normal" micropacket is typically comprised of 32 data bytes and 64 bits of control information. (See col. 9, lines 9, 10, col. 14, lines 46-48).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Collins et al. (US-6031847) in view of Capowski et al. (US-5513377).

Claim 8:

"a. measuring the clock period of the clock channel signal;"

Collins teaches to implement the first step of the clock edge placement, delay stack 313 measures the clock period. (See col. 12, lines 35,36).

"b. determining a clock offset value to properly sample received data from each data channel;"

Collins teaches to implement the second step of the clock edge placement, a clock offset tap decoder 1004, then divides the measured clock period by four.

"c. performing phase correction of all data channels to the common clock channel by aligning any data edge to any clock edge;"

Collins teaches clock edge placement results in the edges of the clock signal being placed such that the deskewed data emerging from the outputs (e.g., outputs d0-d3) of the receiver can be sampled synchronous with the clock signal's rising and falling edges (aligning any data edge to any clock edge). (See col. 14, lines 54-59).

"d. identifying data bit zero phase alignment;"

Collins suggests of the identification of data bit zero alignment in that the ping sequence, where all the channels 0-3 are driven high, sends logical ones down each of the channels 0-3 and into each respective delay stack 310-313. The "edge" (bit zero) of the ping sequence is synchronous in time across each of the channels (e.g., at the transmitter 301 end). Collins teaches a "1" indicates that particular latch registers a

logical one, indicating the ping sequence has rippled past its input (a phase leading condition), while a "0" indicates the ping sequence has not yet reached that particular latch (a phase lagging condition). (See col. 11, lines 13-36).

"e. adjusting a write location to maintain proper bit ordering."

Collins does not explicitly teach of adjusting a write location for the proper ordering of bits. Collins does teach the delay stack 310 includes a ripple decoder 601, a plurality of latches 602-606, a delay line 615, and a tap select multiplexer 620. Capowski teaches in an analogous art that byte synchronization starts by coupling the phase aligned data (now 2 bits wide) into a shift register 33 whose outputs are coupled to multiplexer 35. The deserializer data output for a particular data line is monitored for the expected timing pattern (X 0 1 0 where X is a don't care) to determine the proper order of the received data. If at any time a zero is detected in the bit 3 position the multiplexer is incremented thus moving the byte boundary by one bit time (adjusting a write location). It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjusting a write location using Capowski's shift register/mutiplexer circuit in Colins's latch/mutiplexer circuit. The artisan would be motivated to do so because this function allows synchronization of data lines skewed by more than an entire bit time.

8. Claim 9-12, 19 and 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Collins et al. (US-6031847) in view of Koyanagi et al (US-6636993).

Claim 9:

Collins teaches a parallel data transmission and reception system 300 includes a transmitter 301 (source) coupled to a receiver 302 (destination nodes) via communications channels (interconnect medium) 0 through 3 and functions by deskewing the four bit data words conveyed by channels 0-3 as they arrive (deskew a parallel data link, plurality of channels). (See col. 6, lines 27-31, 39, 40). Collins also teaches in step 1304, the transmitter (source) sends a normal micropacket to the receiver along with a normal clock signal (link clock). A "normal" micropacket is typically comprised of 32 data bytes ("M" bits) and 64 bits of control information. (See col. 9, lines 9, 10, col. 14, lines 46-48). Collins discloses a dynamic skew compensation circuit (DSC), including a receiver, a plurality of channel inputs built into the receiver, and a delay stack structure coupled to the plurality of channel inputs. Each delay stack deskews each communications channel with respect to the others (compensates for skew). (See col. 4, lines 29-46). Collins further teaches the clock edge placement results in the edges of the clock signal being placed such that the deskewed data emerging from the outputs (e.g., outputs d0-d3) of the receiver can be sampled synchronous with the clock signal's rising and falling edges (center the link clock edge with respect to the data bits). (See col. 14, lines 54-59). Collins does not explicitly teach of a plurality of DCS modules however, Koyanagi does teach in an analogous art an automatic deskew system 100 that includes a plurality of deskew subsystems 192 and 180 (DSC modules), and a deskew controller 135 (Bundle Interface Module). (See col. 3, lines 58, 59). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Collins's dynamic skew compensation circuit (DSC) could

be modified, as suggested by Koyanagi, to include a plurality DSC modules in creating a DSC bundle. The artisan would be motivated to do so for this would increase the number of parallel communication channels and thus data throughput in a digital system.

Claim 10 and 11:

Collins teaches the system of the present invention functions in the same manner whether the communications channels are fiber optic (claim 11) or metal (claim 10). (See col. 7, lines 55-57).

Claim 12:

Collins discloses a dynamic skew compensation circuit (DSC), including a receiver, a plurality of channel inputs built into the receiver, and a delay stack structure coupled to the plurality of channel inputs as disclosed in the discussion of claim 9, above. Collins also teaches of a delay stack 313, for the clock signal (clock channel for the DSC). Collins further discloses delay stack 313, and hence, channel 3, convey the clock signal CLK for system 300. The clock signal is transmitted across one of the communications channels (channel 3 in the present example) and is used in sampling the data on the rest of the communications channels.

Claim 19:

The office interprets a cold training sequence (CTS) as a protocol which provides a method for forcing a DSC Module training sequence after a system power-up or reset or an unrecoverable link error. Collins teaches at system 300 power up, transmitter 301 sends normal micropackets alternating with training micropackets (cold training

sequence) until receiver 302 is properly trained and is ready for normal operation. (See col. 14, lines 1-3).

Claim 20:

The office interprets a warm training sequence (WTS) performs a periodic training sequence on all data channels. Collins teaches a WTS in step 1303, the transmitter sends another training micropacket to retrain each of the delay stacks. This second training micropacket is sent immediately after the first training micropacket sent in step 1302. (See col. 14, lines 37-40).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Computer Technology Review, June 2001, by Mark Evans, "Ultra320 SCSI Meets The Challenges"

The operation of the Ultra320 SCSI device is disclosed where training pattern is discussed.

Gigabyte Systems Network, GSN Technical Overview, 11/5/98, by Steve Epp.

The interconnect standard, GSNTM, is discussed in detail with respect to HIPPI-800 compatibility. Training sequences are also discussed along with link connecting material and skew compensation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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